REMARKS

Claims 1-8 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lui (U.S. Patent No. 6,391,761) in view of Bothra, et al. (U.S. Patent No. 6,221,759). Claims 9, 10 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lui in view of Bothra, et al. and further review of Nashner, et al. (U.S. Patent No. 6,465,358). Claims 11-13 and 15-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lui in view of Bothra, et al. and further in view of Liu, et al. (U.S. Patent No. 6,323,121). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

The applicants thank Examiner Nguyen for her helpful comments during the telephone interview conducted with the undersigned on May 5, 2003. In accordance with that interview, the claims are amended to specify that the protective layer set forth in the claim fills the via hole and extends across the via hole. It is believed that this language distinguishes the conformal layer 78 shown in Lui. With reference to the Examiner's response to the applicants' previous Amendment, it is stated that Lui satisfies the claimed limitation "filling the via hole" because layer 78 fills the via hole. It is also stated that the claims do not require that the protective layer fill up the via hole. Accordingly, the clarifying claim language specifies that the protective layer extends across the via hole. It is believed that this new claim language meets the suggestion made by the Examiner that the claims specify that the via hole is filled up by the protective layer.

With the clarifying claim amendments, it is believed that the claims patentably distinguish the cited prior art. None of the references, taken alone or in any combination, teach or suggest the invention set forth in the amended claims. That is, none of the references, taken alone or in combination, teach or suggest the applicants' claimed protective layer filling the via hole and extending across the via hole. Accordingly, it is believed that the claims are allowable over the cited references, and reconsideration of the rejections of the claims is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached pages are captioned "Version with Markings to Show Changes Made."

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the Specification

Please delete the paragraph at page 6, lines 13-17.

In the Claims

1. (Twice Amended) A method of forming an interconnection line in a semiconductor device comprising:

forming a first etching stopper on a lower conductive layer which is formed on a semiconductor substrate;

forming a first interlayer insulating layer on the first etching stopper;

[forming a second etching stopper on the first interlayer insulating layer;]

forming a second interlayer insulating layer [on]over the [second]first etching stopper;

etching the second interlayer insulating layer[, the second etching stopper,] and the first interlayer insulating layer sequentially using the first etching stopper as an etching stopping point to form a via hole aligned with the lower conductive layer;

forming a protective layer to protect a portion of the first etching stopper exposed at the bottom of the via hole, the protective layer filling the via hole and extending across the via hole;

[etching a portion of the second interlayer insulating layer adjacent to the via hole using the second etching stopper as an etching stopping point to form a trench connected to the via hole;]

removing the protective layer;

removing the portion of the first etching stopper positioned at the bottom of the via hole; and

forming an upper conductive layer that fills the via hole and the trench and is electrically connected to the lower conductive layer.

6. (Amended) The method of claim [1] 19, wherein the second etching stopper is formed of at least one of silicon nitride and silicon carbide.

Please add the following new claims.

19. (New) The method of claim 1, further comprising forming a second etching stopper on the first interlayer insulating layer.

20. (New) The method of claim 19, wherein the etching step further comprises etching the second etching stopper with the second interlayer insulating layer and the first interlayer insulating layer using the first etching stopper as an etching stopping point to form the via hole aligned with the lower conductive layer.

21. (New) The method of claim 19, further comprising etching a portion of the second interlayer insulating layer adjacent to the via hole using the second etching stopper as an etching stopping point to form a trench connected to the via hole.

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